This listing of claims will replace all prior versions, and listings, of the claims in this application:

Listing of Claims

Claims 1-12 (canceled)

Claim 13 (currently amended): A pre-decimated integrator filter section, comprising:

a data rate change component; ~~and~~

a first integrator structure comprising at least one recursive integrator stage, said first integrator structure receiving data at a rate established by said data rate change component, said first integrator structure modifying data received from said data rate change component; and

a read only memory device, said read only memory device being used by said first integrator structure to modify data received from said data rate change component;

wherein the pre-decimated integrator filter section outputs data equivalent to data that would be output by a post-decimated integrator filter section having an equal number of integrator stages.

Claim 14 (original): The pre-decimated integrator filter section according to Claim 13, further comprising a second integrator structure having one or more integrator stages.

Claim 15 (previously presented): The pre-decimated integrator filter section according to Claim 13, wherein said first integrator structure comprises a recursive integrator stage and a plurality of multipliers.

Claim 16 (original): The pre-decimated integrator filter section according to Claim 13, wherein said data rate change component comprises a serial to parallel converter.

Claim 17 (canceled)

Claim 18 (original): The pre-decimated integrator filter section according to Claim 13, wherein said first integrator structure modifies data received from said data rate change component by applying coefficients stored in a look-up table.

Claim 19 (previously presented): The pre-decimated integrator filter section according to Claim 13, wherein said first integrator structure comprises a plurality of reduced rate parallel signal paths with a recursive integrator stage and a plurality of coefficient multipliers for each path.

Claim 20 (currently amended): A method of performing a pre-decimated cascaded integration in a filter section, comprising the steps of:

changing the data rate of data being received by an integrator structure;

performing a first integration procedure on data received at the changed data rate, wherein the first integration procedure includes at least one recursive integrator stage;

executing a second integration procedure on data output by said first integration procedure, wherein the second integration procedure includes a plurality of parallel recursive integrator stages ~~at least one additional recursive integrator stage~~; and

outputting data equivalent to data that would be output by a post-decimated cascaded integrator having an equal number of integrator stages.

Claim 21 (canceled)

Claim 22 (original): A method according to Claim 20, wherein said changing step comprises converting a received serial data stream to a parallel signal having a plurality of parallel paths and decimating the received data by a factor equal to the number of parallel paths.

Claim 23 (original): The method according to Claim 20, wherein said performing step further comprises modifying the received data by multiplication by determined coefficients.

Claim 24 (original): The method according to Claim 20, wherein said performing step comprises a step of accessing a memory device, data held by said memory device being used during said performing step to modify data received from said data rate change component.

Claim 25 (original): The method according to Claim 20, wherein said performing step includes a combining procedure further modifying data received at the changed data rate.

Claims 26-34 (canceled)

Claim 35 (new): A method of performing a pre-decimated cascaded integration in a filter section, comprising the steps of:

changing the data rate of data being received by an integrator structure;

performing a first integration procedure on data received at the changed data rate, wherein the first integration procedure includes at least one recursive integrator stage and wherein said performing step further comprises modifying the received data by multiplication by determined coefficients;

executing a second integration procedure on data output by said first integration procedure, wherein the second integration procedure includes at least one additional recursive integrator stage; and

outputting data equivalent to data that would be output by a post-decimated cascaded integrator having an equal number of integrator stages.

Claim 36 (new): A method according to Claim 35, wherein said executing step comprises processing received data with a plurality of parallel recursive integrator stages.

Claim 37 (new): A method according to Claim 35, wherein said changing step comprises converting a received serial data stream to a parallel signal having a plurality of parallel paths and decimating the received data by a factor equal to the number of parallel paths.

Claim 38 (new): The method according to Claim 35, wherein said performing step comprises a step of accessing a memory device, data held by said memory device being used during said performing step to modify data received from said data rate change component.

Claim 39 (new): The method according to Claim 35, wherein said performing step includes a combining procedure further modifying data received at the changed data rate.

Claim 40 (new): A pre-decimated integrator filter section, comprising:

a data rate change component; and

a first integrator structure comprising at least one recursive integrator stage, said first integrator structure receiving data at a rate established by said data rate change component, said first integrator structure modifying data received from said data rate change component by applying coefficients stored in a look-up table;

wherein the pre-decimated integrator filter section outputs data equivalent to data that would be output by a post-decimated integrator filter section having an equal number of integrator stages.

Claim 41 (new): The pre-decimated integrator filter section according to Claim 40, further comprising a second integrator structure having one or more integrator stages.

Claim 42 (new): The pre-decimated integrator filter section according to Claim 40, wherein said first integrator structure comprises a recursive integrator stage and a plurality of multipliers.

Claim 43 (new): The pre-decimated integrator filter section according to Claim 40, wherein said data rate change component comprises a serial to parallel converter.

Claim 44 (new): The pre-decimated integrator filter section according to Claim 40, further comprising a read only memory device, said read only memory device being used by said first integrator structure to modify data received from said data rate change component.

Claim 45 (new): The pre-decimated integrator filter section according to Claim 40, wherein said first integrator structure comprises a plurality of reduced rate parallel signal paths with a recursive integrator stage and a plurality of coefficient multipliers for each path.

Claim 46 (new): A pre-decimated integrator filter section, comprising:

a data rate change component; and

a first integrator structure comprising a plurality of reduced rate parallel signal paths with a recursive integrator stage and a plurality of coefficient multipliers for each path, said first integrator structure receiving data at a rate established by said data rate change component, said first integrator structure modifying data received from said data rate change component;

wherein the pre-decimated integrator filter section outputs data equivalent to data that would be output by a post-decimated integrator filter section having an equal number of integrator stages.

Claim 47 (new): The pre-decimated integrator filter section according to Claim 46, further comprising a second integrator structure having one or more integrator stages.

Claim 48 (new): The pre-decimated integrator filter section according to Claim 46, wherein said data rate change component comprises a serial to parallel converter.

Claim 49 (new): The pre-decimated integrator filter section according to Claim 46, further comprising a read only memory device, said read only memory device being used by said first integrator structure to modify data received from said data rate change component.

Claim 50 (new): The pre-decimated integrator filter section according to Claim 46, wherein said first integrator structure modifies data received from said data rate change component by applying coefficients stored in a look-up table.